IN THE CLAIMS

Please amend the claims as follows:

1. (Amended) A method comprising the steps of:

a) identifying at least one statement within a register transfer level (RTL) synthesizable source code; and

b) synthesizing the source code into a gate-level netlist including at least one instrumentation signal, wherein the instrumentation signal is indicative of an execution status of the at least one statement.

5. (Amended) A method of generating a gate level design, comprising the steps of:

a) creating an instrumentation signal associated with at least one synthesizable statement contained in a register transfer level (RTL) synthesizable source code; and

b) synthesizing the source code into a gate-level design having the instrumentation signal.

12. (Amended) A method of generating a gate-level netlist, comprising the steps of:

a) receiving register transfer level (RTL) synthesizable source code including synthesizable statements;

b) inserting a unique local variable assignment statement into the source code for each branch of code having a list of at least one sequential statement, wherein

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the unique local variable assignment statement is adjacent to at least one statement within the list;

c) inserting a corresponding instrumentation signal assignment statement into the source code for each of the inserted local variables, wherein the instrumentation signal is assigned a value of the corresponding unique local variable; and

d) synthesizing the source code into a gate-level design including the instrumentation signals.

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16. (Amended) A method of generating a gate level netlist, comprising the steps of:

a) receiving register transfer level (RTL) synthesizable source code including synthesizable statements;

b) modifying the source code to generate a corresponding sampled version of each signal event in a selected process;

c) modifying the source code to duplicate the selected process;

d) replacing each occurrence of a selected signal event with the corresponding sampled version in the duplicated process;

e) replacing each list of sequential statements within an executable branch of the duplicated process with a unique variable assignment statement;

f) modifying the duplicated process to include an instrumentation signal assignment for each unique variable; and

g) synthesizing the modified source code into a gate-level design.

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20. (Amended) A method of debugging a gate-level design including the steps of:

a) setting a breakpoint at a selected statement of a register transfer level (RTL) synthesizable source code;

b) inserting a local variable assignment statement adjacent to at least one statement in a list of sequential statements, wherein the list corresponds to an executable branch of the source code including the selected statement;

c) modifying the source code to include an instrumentation signal assignment statement for the local variable; and

d) generating a gate-level design from the modified source code.

REMARKS

This amendment is submitted in response to an Office Action mailed February 01, 2000. Applicant respectfully requests reconsideration of the subject application as amended herein.

Claims 1-33 remain in the present application.

The specification has been amended to correct previously undetected informalities.

Accompanying this amendment is a Request to Approve Drawing Changes. Figures 10, 11, 13 and 16 have been amended to correct previously undetected informalities.

No new matter has been added.